AMENDMENTS TO THE CLAIMS:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

Claims 1-9 (canceled)

10. (Currently Amended) ~~The data processor of Claim 7, wherein~~A data processor comprising:

a CPU;

an internal memory accessible by said CPU; and

a control circuit capable of responding to a particular access request issued by said CPU to control a block transfer, in which said internal memory is used as a first transfer object;

a cache memory coupled to a first bus which is coupled to said CPU, said internal memory, and said control circuit; and

a bus interface controller connected to said control circuit, and operable to perform interface control for a second transfer object,

wherein a set of instructions for said CPU includes a particular instruction for making said CPU issue the particular access request,

the particular instruction has an address field,

when an address specified by the address field is a logical address mapped to said internal memory, the address is set as one of a transfer source address or a transfer destination address of the block transfer, and

a transfer source address or transfer destination address for said second transfer object of the block transfer is a physical address corresponding to a logical address of said address field,

said internal memory is assigned a cache non-object address for said cache memory,

the ~~set of instructions for said CPU~~ particular instruction includes a first cache memory-operating instruction, and

when the logical address specified by the address field directs a cache object address for said cache memory, the first cache memory-operating instruction causes an operation of making said cache memory retain data of an external memory associated with the physical address corresponding to the different logical address, at a cache object address specified by the logical address.

11. (currently amended) The data processor of Claim 10, wherein the particular instruction includes a second cache memory-operating instruction, and

when the logical address specified by the address~~addressing~~ field directs a cache object address and a cache hit is detected at a data location specified by the logical address and a cache entry associated with the cache hit is dirty, the second cache memory-operating instruction causes an operation of writing back to the external memory.

12. (currently amended) The data processor of Claim 10, wherein the particular instruction has an operation code identical to that of the first cache memory-operating instruction, and sets the cache non-object address of the address~~addressing~~ field as the destination address.

13. (currently amended) The data processor of Claim 11, wherein the particular instruction has an operation code identical to that of the second cache memory-operating instruction, and sets the cache non-object address of the address~~addressing~~ field as the source address.

Claims 14-20 (canceled)

21. (new) The data processor of Claim 10, wherein said control circuit is capable of performing memory control in regard to a cache hit and a cache miss with respect to said cache memory.